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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,518	11/09/2001	Vincent K. Chan	ATI.0100750	3080

34456 7590 12/16/2003

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EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,518	CHAN ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 41-46* is/are pending in the application.

4a) Of the above claim(s) *1-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-39 and 41-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of species 4 in the paper dated 10/15/03 is acknowledged.

Applicant cited claims 35-38 and 41-46 as the claims readable thereon and also amended many of the claims. In light of these amendments, the examiner will examine all the pending claims 19-39, and 41-46.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19, 20, 23-26, 29-32, 35-39, and 43-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Degani et al., US Patent 5,646,828.

Degani teaches an multi chip module electronic package, comprising:

a first semiconductor device (19 or 20) capable of enabling functionality associated with a first circuit segment of an integrated circuit design and including a set of first device interconnect pads;

a second semiconductor device (18) capable of enabling functionality associated with a second circuit segment of the integrated circuit design and including a set of second device interconnect pads; and

a plurality of device interconnect members, each one of said device interconnect members being electrically connected directly between one of said first device interconnect pads and a corresponding one of said second device interconnect pads (Figure 7).

Regarding claims 20 and 32, Degani teaches the first semiconductor device as being capable of enabling functionality associated with a first functional block of the integrated circuit design; and the second semiconductor device as being capable of enabling functionality associated with a second functional block of the integrated circuit design (Figure 7).

With respect to claims 23-26, 29-30, 35-37, 43 and 44, Degani teaches the use of solder balls (figure 7).

As to claim 31, Degani teaches the use of an interposer circuit (71) including a dielectric substrate and an array of routing elements attached to the dielectric substrate; and further comprising a set of package-level interconnect pads; and a plurality of package-level interconnect members (74), each one of said package-level interconnect members being electrically connected between one of the said package-level interconnect pads of the second semiconductor device and a corresponding one of said routing elements of the interposer circuit (figure 7).

Regarding the examiners use of the PWB of Degani as the interposer of the present claims, a few points will be made.

One, PWB are inherently made of insulating materials and the present specification's definition of dielectric substrate as including flexible or plastic BGAs (page 8, lines 25+), which inherently are made of insulating materials. Therefore, the examiner is assuming the word dielectric is intended to mean insulating and consequently that a PWB is a dielectric substrate having an array of routing elements thereon.

Two, the examiner further interpreted PWB as being an interposer. An interposer is a substrate that electrically connects one substrate to another. As seen in Figure 8 of Degani and as stated on page 8, lines 9+, the PWB can and is used to electrically connect the chips to another substrate.

In re claim 38 and 45, Degani teaches the interposer circuit is a flip-chip interposer circuit; and each one of said package-level interconnect members is a solder-type interconnect member (Figure 8).

Regarding claims 39 and 46, Degani teaches the interposer circuit is a wire-bond interposer circuit; and each one of said package-level interconnect members is a conductive wire (Figure 2).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-21, 23-27, 29, and 30 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ference et al., US Patent 6,225,699 (figure 1).

Regarding claims 20 and 27, Ference teaches the first semiconductor device as being capable of enabling functionality associated with a first functional block of the integrated circuit design; and the second semiconductor device as being capable of enabling functionality associated with a second functional block of the integrated circuit design (Figure 1).

With respect to claim 21, Ference the first device as being a DRAM device and the second device as being a logic device (1, 20+).

As to claims 23-26, 29 and 30, Ference teaches the use of solder balls as the interconnect member (figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21, 22, 27, 28, 33, 34, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al., US Patent 5,646,828, as applied to claims 19, 20, 23-26, 29-32, 35-39, and 43-46 above.

Regarding claims 21, 27, 33 and 41, while Degani fails to teach the use of a DRAM device and a logic device as the first and second devices, it would have been obvious to a skilled artisan to use a DRAM and logic device because they are conventionally known in the art devices. The use of conventional materials to perform

there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

With respect to claims 22, 28, 34 and 42, while Degani fails to teach the use of different semiconductor substrate materials for the first and second devices, it would have been obvious to a skilled artisan to use a different materials for each device because it is a conventionally known in the art design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)).

Claims 22, 28, 31-39 and 41-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ference et al., US Patent 6,225,699, as applied to claims 19-21, 23-27, 29, and 30 above, and further in view of Degani et al., US Patent 5,646,828.

Regarding claims 22, 28, 34 and 42, while Ference fails to teach the use of different semiconductor substrate materials for the first and second devices, it would have been obvious to a skilled artisan to use a different materials for each device because it is a conventionally known in the art design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)).

With respect to claim 31, while Ference teaches a package, substrate or third chip as reference number 20, Ference fails to teach an interposer circuit including a dielectric substrate and an array of routing elements attached to the dielectric substrate; and further comprising a set of package-level interconnect pads; and a plurality of package-level interconnect members, each one of said package-level interconnect

members being electrically connected between one of the said package-level interconnect pads of the second semiconductor device and a corresponding one of said routing elements of the interposer circuit.

Degani (figure 7) teaches the use of an interposer circuit (71) including a dielectric substrate and an array of routing elements attached to the dielectric substrate; and further comprising a set of package-level interconnect pads; and a plurality of package-level interconnect members (74), each one of said package-level interconnect members being electrically connected between one of the said package-level interconnect pads of the second semiconductor device and a corresponding one of said routing elements of the interposer circuit.

Regarding the examiners use of the PWB of Degani as the interposer of the present claims, a few points will be made.

One, PWB are inherently made of insulating materials and the present specification's definition of dielectric substrate as including flexible or plastic BGAs (page 8, lines 25+), which inherently are made of insulating materials. Therefore, the examiner is assuming the word dielectric is intended to mean insulating and consequently that a PWB is a dielectric substrate having an array of routing elements thereon.

Two, the examiner further interpreted PWB as being an interposer. An interposer is a substrate that electrically connects one substrate to another. As seen in Figure 8 of Degani and as stated on page 8, lines 9+, the PWB can and is used to electrically connect the chips to another substrate.

Regarding claim 32, Ference teaches the first semiconductor device as being capable of enabling functionality associated with a first functional block of the integrated circuit design; and the second semiconductor device as being capable of enabling functionality associated with a second functional block of the integrated circuit design (Figure 1).

With respect to claims 33 and 41, Ference the first device as being a DRAM device and the second device as being a logic device (1, 20+).

As to claims 35-37, 43 and 44, Ference teaches the use of solder balls as the interconnect member (figure 1).

In re claims 38 and 45, Ference teaches a flip chip interposer and the package-level interconnect members as being solder-type interconnect members (figure 1).

Regarding claims 39 and 46, Ference teaches a wire-bond interposer and the package-level interconnect members as being conductive wire interconnect members (figure 15).

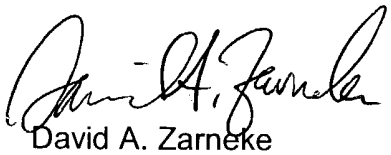
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,977,640 to Bertin et al. and US Patents 6,160,715 and 6,154,370 both to Degani et al., are cited as teaching the very similar to the present invention. Particularly claim 19.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703)-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-6789.



David A. Zarneke
Primary Examiner
December 4, 2003